REMARKS/ARGUMENTS

Status of Claims

Claims 1 to 41 are currently pending in the application.

Applicant gratefully acknowledges the Examiner's indication that claims 1 to 32 are allowable.

Amendments to Claims

Claim 33 has been amended to recite "a set of circuit elements connected to cause sequential transitions of any mixed-signal output that is in a respective off state or in the respective analog range towards a respective on state during [[a]] the first control state, and to cause sequential transitions of any mixed-signal output that is in a respective on state or in the respective analog range towards a respective off state during [[a]] the second control state", where the square bracketed indefinite article "a" has been deleted from the claim and replace with the definite article "the". This amendment is to emphasize that the first and second control states recited in this particular limitation of claim 33 are the same first and second control states as recited in the earlier limitation of the claim, "at least one control input defining at least a first control state and a second control state".

Claim 40 has been amended to recite "A method for processing a set of mixed-signal outputs, each mixed-signal output characterized by a digital state and an analog state, the method comprising:

detecting when a particular mixed-signal output has reached a digital state;

upon detecting that a particular mixed-signal output has reached [[a]] the digital state, securing the particular mixed-signal output to an appropriate reference".

Further defining "each mixed-signal output characterized by a digital state and an analog state" clarifies that a mixed-signal output is a signal that is characterized by both a digital state and an analog state.

35 U.S.C. § 102 Rejections

Controlling case law has frequently addressed rejections under 35 U.S.C. § 102. "For a prior art reference to anticipate in terms of 35 U.S.C. Section 102, **every element** of the claimed invention **must** be **identically** shown in a single reference." Diversitech Corp. v. Century Steps, Inc., 850 F.2d 675, 677, 7 U.S.P.Q.2d 1315, 1317 (Fed. Cir. 1988; emphasis added). The disclosed elements must be arranged as in the claim under review. See Lindemann Machinefabrik v. American Hoist & Derrick Co., 730 F.2d 1452, 1458, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984). If any claim element or step is absent from the reference that is being relied upon, there is **no** anticipation. Kloster Speedsteel AB v. Crucible, Inc., 793 F.2d 1565, 230 U.S.P.Q. 81 (Fed. Cir. 1986; emphasis added). The following analysis of the present rejections is respectfully offered with guidance from the foregoing controlling case law decisions.

The Examiner has rejected claims 33 to 35 under 35 U.S.C. 102(b) as being anticipated by Tanaka (JP 55052596).

With regard to claim 33, the Examiner has alleged that Tanaka discloses a circuit comprising "at least one control input defining at least a first control state and a second control state; a plurality of mixed-signal outputs each characterized by a respective on state, a respective off state and a respective analog range; a set of circuit elements connected to cause sequential transitions of any mixed-signal output that is in a respective off state or in the respective analog range towards a respective on state during a first control state and to cause sequential transitions of any mixed-signal output that is in a respective on state or in the respective analog range towards a respective off state during a second control state."

The Examiner equates "a respective analog range" as recited in claim 33 with a "tri-state" output of blocks 20n in Figure 4 of Tanaka. Applicant submits that simply because a particular device may be a tri-state device, there is no reason to automatically assume that a tri-state output has an analog range. A tri-state device typically has three outputs, 0, 1 and Z where Z is a high impedance output. Whereas 0 and 1 are definite outputs, Z may be considered a lack of a definite output, similar to an open circuit, which provides the high impedance output.

Furthermore, Applicant submits that blocks 20n in Figure 4 as disclosed in Tanaka illustrate a cascade of dynamic latches/shift-registers, each dynamic latch/shift-register configured to drive immediately to a 0 or 1 value, saturate, and stay at the 0 or 1 value when the dynamic latch/shift-register output goes tri-state. There is no suggestion or disclosure in the figures cited by the Examiner that indicates that the output of any of blocks 20n has a "respective analog range".

As Tanaka does not disclose a signal having an analog range, Applicant submits that Tanaka consequently does not disclose a "mixed-signal output" as recited in claim 33, which is a signal "characterized by a respective on state, a respective off state, and a respective analog range".

The Examiner has alleged that that clock signal ϕ as disclosed in Figure 4 of Tanaka is equivalent to "at least one control input defining a first control state and a second control state" as recited in claim 33. Applicant submits that clock signal ϕ is not the same as a control input defining a first control state and a second control state. The clock signal has two states, specifically a HI and a LO, but Applicant submits that these HI and LO values are not "control states" in the manner recited in claim 33. Examples of the first and second control states of the control input recited in claim 33 are a state during which a mixed signal output is transitioned from off to on and a state during which a mixed signal output is transitioned from on to off. Looking at the timing diagram of Figure 7 of Tanaka for example, Applicant submits that the durations of the HIs and LOs of clock signal ϕ do not directly correspond to an off state transitioning to an on state or a on state transitioning to an off state. Therefore, clock signal ϕ is not the same as a control input defining a first control state and a second control state.

For at least the above reasons, Applicant submits that Tanaka does not disclose all the limitations recited in claim 33. Applicant submits that as Tanaka does not disclose all of the limitations of claim 33, claim 33 is not anticipated.

Claims 34 and 35 are dependent upon claim 33. For at least their dependence upon claim 33, Applicant submits that Tanaka does not include all the limitations of claims 34 and 35 and therefore, claims 34 and 35 are not anticipated.

Applicant respectfully requests for the Examiner to reconsider and withdraw the anticipation rejection of claims 33 to 35.

The Examiner has rejected claims 36 to 41 under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (U.S. Patent No. 6,515,648).

With regard to claim 36, the Examiner alleges that Tanaka et al. discloses a method for "dynamically determining if a particular output of a set of mixed-signal outputs representing a mixed signal code is outputting an analog value, the method comprising: receiving at least one neighbouring mixed-signal outputs; determining if the neighbouring mixed-signal outputs are consistent with the particular mixed-signal output being an analog value for the mixed-signal code".

The Examiner equates "a set of mixed-signal outputs representing a mixed signal code " as recited in claim 36 with the outputs of clocked inverter circuits 2n1, i.e. 211, 221, 231, 241, 251 in Figure 2 of Tanaka et al. Applicant submits that there is no suggestion or disclosure in Tanaka et al. that the outputs of the clocked inverter circuits 2n1 form a mixed-signal code. These outputs represent a set of respective outputs from the clocked inverter circuits 2n1, which are then provided to inverter circuits 2n2.

The Examiner further equates "receiving at least one neighbouring mixed-signal outputs" as recited in claim 36 with inverter circuit 2n2, i.e. 212, 222, 232, 242, 252 in Figure 2 of Tanaka et al. receiving the output of clocked inverter circuits 2n1. Applicant submits that the outputs of the clocked inverter circuits 2n1 and the inverter circuits 2n2 are not "neighbouring mixed-signal outputs" as recited in claim 36. The inverter circuits 2n2 are connected serially with the clocked inverter circuits 2n1 and invert the output of the clocked inverter circuits 2n1. When considering the claim as a whole, it must be considered that the step of "determining if the neighbouring mixed-signal outputs are consistent with the particular mixed-signal output being an analog value for the mixed-signal code" is being performed with regard to a mixed signal output and a neighbouring mixed signal output. In the scenario that the Examiner has raised, since a signal output from the inverter circuits 2n2 is only an inverted form of the output from clocked inverter circuits 2n1, there is no point in "determining if the neighbouring mixed-signal outputs are

consistent with the particular mixed-signal output being an analog value for the mixed-signal code" because the outputs would definitely be consistent.

The Examiner further alleges that "determining if the neighbouring mixed-signal outputs are consistent with the particular mixed-signal output being an analog value for the mixed-signal code" as recited in claim 36 is equivalent to being able to determine that an output of clocked inverter circuit 2n1 is a tri-state value based on "the output of 2n2 is unchanged when 2n1 is in tri-state". Applicant submits that there is no suggestion or disclosure of a "determining" step in Tanaka et al. that determines if neighbouring mixed-signal outputs are consistent with a particular mixed-signal output being an analog value.

In addition, Applicant submits that there is no suggestion or disclosure that the output of either of clocked inverter circuits 2n1 or inverter circuits 2n2 have an analog output. As mentioned above, there is no reason to automatically assume that a tri-state output has an analog range, and the Examiner has not provided a sufficient reasoning to suggest that either of the clocked inverter circuits 2n1 or inverter circuits 2n2 have an analog output.

For at least the above reasons, Applicant submits that Tanaka et al. does not disclose all the limitations recited in claims 36. Applicant submits that as Tanaka et al. does not disclose all of the limitations of claim 36, claim 36 is not anticipated.

Claims 37 to 39 are dependent upon claim 36. For at least their dependence upon claim 36, Applicant submits that claims 37 to 39 are not anticipated by Tanaka et al.

With regard to claim 40, the Examiner alleges that Tanaka et al. discloses "detecting when a particular mixed-signal has reached a digital state". Amended claim 40 recites that each mixed-signal output is "characterized by a digital state and an analog state". There is no suggestion or disclosure in Tanaka et al. that an output of inverter circuits 2n2 is a mixed-signal output that is characterized by both an analog state and a digital state. Therefore, as Tanaka et al. does not suggest or disclose an analog state, outputs of inverter circuit 2n2 must always be in a digital state and therefore there is no reason for a need to detect when a signal output has reached a digital state, as recited in claim 40.

For at least the above reasons, Applicant submits that Tanaka et al. does not disclose all the limitations recited in claim 40. Applicant submits that as Tanaka et al. does not disclose all of the limitations of claim 40, claim 40 is not anticipated.

Claim 41 is dependent upon claim 40. For at least its dependence upon claim 40, Applicant submits that claim 41 is not anticipated by Tanaka et al.

Furthermore, claim 41 recites steps of "receiving at least one neighbouring mixed-signal output" and "determining if the neighbouring mixed-signal outputs are consistent with the particular mixed-signal output being a digital state for the mixed-signal code", which are similar to steps of claim 36, except the expression "analog value" in claim 36 is "digital state" in claim 41. For similar reasons as discussed above with regard to claim 36, Applicant submits that Tanaka et al. does not disclose all the limitations of claim 41, in particular those dealing with a "neighbouring mixed-signal output".

Applicant respectfully requests for the Examiner to reconsider and withdraw the anticipation rejection of claims 36 to 41.

In view of the foregoing, early favorable consideration of this application is earnestly solicited.

Respectfully submitted,

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